REMARKS

At the outset, Applicants thank the Examiner for courtesies extended to Applicants' representatives in a personal interview on August 10, 2004 and for the thorough review and consideration of the subject application. The Final Office Action of April 27, 2004 has been received and its contents carefully reviewed.

Claims 1, 14, 20, and 21 are hereby amended. Accordingly, claims 1-21 are currently pending. Reexamination and reconsideration of the pending claims is respectfully requested.

In the Final Office Action of April 27, 2004, the Examiner rejected claims 1-22 and 24 under 35 U.S.C. § 103(a) as being unpatentable over the related art illustrated in Figures 1-6 in view of Ito et al. (U.S. Patent No. 5,748,179) or Suzuki et al. (U.S. Patent No. 5,739,880) or Lim (U.S. Patent No. 6,429,908); and objected to claim 23 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicants appreciate the indication of allowable subject matter in claim 23. However, the rejection of claims 1-22 and 24 under 35 U.S.C. § 103(a) as being unpatentable over the related art illustrated in Figures 1-6 in view of Ito et al. or Suzuki et al. or Lim is respectfully traversed and reconsideration is requested.

For purposes of providing a clear prosecution history, Applicants note it appears as though Ito et al., Suzuki et al., and Lim are being used to independently modify the alleged teachings of the related art shown in Figures 1-6 of the present application. Accordingly, Applicants hereby proceed assuming the grounds of rejection for claims 1-22 and 24 could alternately have been set forth as "the related art illustrated in Figures 1-6 in view of Ito et al.," "the related art illustrated in Figures 1-6 in view of Suzuki et al.," or "the related art illustrated in Figures 1-6 in view of Lim."

Claim 1 is allowable over the related art illustrated in Figures 1-6 in view of Ito et al. or Suzuki et al. or Lim in that claim 1 recites a combination of elements including, at least "wherein a first gate transmitting line of the plurality of gate transmitting lines has a first resistance, wherein the plurality of gate transmitting lines other than the first gate transmitting line have a second resistance, and wherein the first resistance is less than the second resistance." Neither the related art shown in Figures 1-6, Ito et al., Suzuki et al., nor Lim, singly or in combination, teach or suggest at least this feature of the claimed invention. Accordingly,

Applicants respectfully submit that claims 2-13, 22, and 24, which depend from claim 1, are also allowable over the related art illustrated in Figures 1-6 in view of Ito et al. or Suzuki et al. or Lim.

Claim 14 is allowable over the related art illustrated in Figures 1-6 in view of Ito et al. or Suzuki et al. or Lim in that claim 14 recites a combination of elements including, at least "a plurality of gate transmitting lines... wherein one of the plurality of gate transmitting lines has a first resistance and wherein the others of the plurality of gate transmitting lines has a second resistance greater than the first resistance." Neither the related art shown in Figures 1-6, Ito et al., Suzuki et al., nor Lim, singly or in combination, teach or suggest at least this feature of the claimed invention. Accordingly, Applicants respectfully submit that claims 15-19, which depend from claim 14, are also allowable over the related art illustrated in Figures 1-6 in view of Ito et al. or Suzuki et al. or Lim.

Claim 20 is allowable over the related art illustrated in Figures 1-6 in view of Ito et al. or Suzuki et al. or Lim in that claim 20 recites a combination of elements including, at least "forming a plurality of gate transmitting lines... wherein one of the plurality of gate transmitting lines has a first resistance and wherein the others of the plurality of gate transmitting lines has a second resistance greater than the first resistance." Neither the related art shown in Figures 1-6, Ito et al., Suzuki et al., nor Lim, singly or in combination, teach or suggest at least this feature of the claimed invention. Accordingly, Applicants respectfully submit that claim 21, which depends from claim 20, is also allowable over the related art illustrated in Figures 1-6 in view of Ito et al. or Suzuki et al. or Lim.

The Examiner cites the related art shown in Figures 1-6 as failing to disclose wherein "one of the gate transmitting lines has a resistance that is less than the other gate transmitting lines (or the gate transmitting lines comprise two resistances) as claimed in claims 1, 14, 20, 22, and 24...." The Examiner attempts to cure the deficiencies of the related art shown in Figures 1-6 by relying upon various teachings of Ito et al., Suzuki et al., and Lim.

Specifically, the Examiner cites Ito et al. as disclosing "that the input wire (Td) to the driving IC (transmitting gate driving signal) comprises a first conductive film (g1) and a second conductive film (d2), and the first conductive film (g1) is formed of low-resistance metal such as Al-Ta or the like and the second conductive film (d2) is formed of low-resistance metal such as Cr or the like. Because the metal Al and Cr are different metal material and that must have

different resistivities and different resistances." Further, the Examiner cites Ito et al. as disclosing "that larger resistance occurs at the gate side and at the drain side would cause the distortion amount of the output waveform of the driving IC is varied every wiring, and this finally causes unevenness of a display image." After citing Ito et al., the Examiner apparently concludes, stating "[t]herefore, it is necessary to reduce the resistance of the signal transmitting lines in order to reduce the signal distortion such as a cross-talk."

The Examiner cites Suzuki et al. as disclosing "that it is necessary to reduce the resistance of the output wiring (i.e., the signal transmitting lines) because the signal waveform propagation delay is dependent on the resistance of the signal transmitting lines such as the gate lines and the capacitance loaded upon the signal transmitting lines such as the gate lines (i.e., the RC constant)." After citing Suzuki et al., the Examiner apparently concludes, stating "[t]herefore, the larger resistance of the signal transmitting line would cause larger signal propagation delay, and that would cause signal waveform distortion, and unevenness of a display image."

Lastly, the Examiner cites Lim as disclosing "that the aluminum... is a low resistance metal and the chromium... is a high resistance conductive metal relatively and that it is conventional."

Concluding the rejection of claims 1, 14, and 20, the Examiner alleges that "it would have been obvious to... arrange one of the gate transmitting lines having different resistances as claimed in claims 1, 14, 20... for preventing the unevenness of a display image, i.e., to reduce the resistance of the signal transmitting lines in order to reduce the signal distortion such as a cross-talk. Applicants respectfully disagree.

It is respectfully submitted that the Abstract of Ito et al. discloses:

> "A liquid crystal display device is provided which reduces the resistance of input wires disposed between a flexible board and driving ICs mounted in a flip-chip style.... The liquid crystal display device includes... plural input wires (Td).... Each input wire includes a first metal layer (g1) in the vicinity of the surface of the substrate, a transparent conductive layer (d1) laminated on the first metal layer... a second metal layer (d2) laminated on the transparent conductive film and connected to the first metal layer... and a protection film (PSV1) covering at least the second metal layer."

Regardless of whether or not Ito et al. discusses any relationship between line resistance and signal distortion, as alleged by the Examiner, Applicants respectfully submit Ito et al. fails to teach or suggest the deficiency of the related art shown in Figures 1-6 (e.g., a liquid crystal display device, or a method of making a liquid crystal display device, that includes a set of gate transmitting lines having different resistances as set forth in claims 1, 14, and 20). To reiterate, claim 1 recites, among other elements, "wherein a first gate transmitting line of the plurality of gate transmitting lines has a first resistance, wherein gate transmitting lines other than the first gate transmitting line have a second resistance, and wherein the first resistance is less than the second resistance;" claim 14 recites, among other elements, "a plurality of gate transmitting lines... wherein the plurality of gate transmitting lines comprise two resistances;" and claim 20 recites, among other elements, "forming a plurality of gate transmitting lines... wherein the plurality of gate transmitting lines comprise two resistances."

Similarly, Suzuki et al. can be reasonably understood to teach at column 12, lines 5-27, that it is "necessary to reduce not only the variation of the wiring resistance, but also the resistance itself of the output wiring" due to the existence of a waveform distortion ultimately brought on by a resistance R of the gate line GL in the effective display portion AR (see Figure 7). However, it cannot be reasonably understood that Suzuki et al., in light of the citation above, teaches or even suggests a liquid crystal display device, or a method of making a liquid crystal display device, that includes a set of gate transmitting lines having different resistances, such that the signals are transmitted without distortion, as claimed in claims 1, 14, and 20 above.

Lastly, Lim teaches at column 3, lines 9-18, that"

> "an active panel includes a repair line... [wherein] all parts of the repair line are formed when the gate electrode is formed. Therefore, the repair line comprises low resistance metal such as Al, AlNd, Mo and Cu so that any signal delay occurring at the detoured data line is significantly reduced."

Accordingly, Applicants respectfully submit that Lim fails to teach or suggest a liquid crystal display device, or a method of making a liquid crystal display device, that includes a set of gate transmitting lines having different resistances as claimed in claims 1, 14, and 20 above.

In light of the above, Applicants respectfully submit that Ito et al., Suzuki et al., and Lim not only fail to teach or suggest what is actually claimed, but actually teach away from the present claimed inventions defined by claims 1, 14, and 20, reiterated above. Accordingly,

Applicants respectfully submit the requisite motivation to combine the references, and arrive at the claimed inventions, is absent. Rather, motivation to combine the cited references as suggested by the Examiner is found only in the present application via the use of impermissible hindsight reasoning.

In the "Response to Arguments" section of the present Office Action, the Examiner appears to respond to the arguments presented above (the arguments presented above are essentially identical to the arguments presented in the Submission under 37 C.F.R. § 1.114, filed on April 15, 2004) merely by duplicating the previously cited teachings of Ito et al., Suzuki et al., and Lim.

Applicants respectfully submit, however, that merely duplicating alleged teachings of individual references fails to address the substance of Applicants' arguments that the combination of the applied references fails to teach or suggest what is actually being claimed. Specifically, reiterating what applied references teach individually does not explain how or why the combination of references suggests each claimed element. According to M.P.E.P. § 707.07(f), the Examiner should, if he or she repeats the rejection, take note of arguments accompanying any of Applicants' traversals of rejection and answer the substance of those arguments. If the Examiner intends to maintain the present rejection, Applicants respectfully request the Examiner address each and every argument as set forth above.

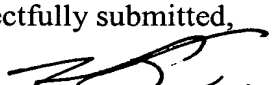
In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

If the Examiner deems that a telephone conversation would further the prosecution of this application, the Examiner is invited to call the undersigned at (202) 496-7500.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Dated: August 18, 2004

Respectfully submitted,

By 

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